Improve the Performance of LC Resonant Clock Distribution Networks Based on Low-Swing Differential Conditional Capturing Flip-Flop

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Abstract: In this paper we introduce a new flip-flop for use in a low swing LC resonant clocking scheme. The proposed low-swing differential conditional capturing flip-flop (LS-DCCFF) operates with a low-swing sinusoidal clock through the utilization of reduced swing inverter at the clock port. The functionality of the proposed flip-flop was verified at extreme corners through simulations with parasitics extracted from layout. The LS-DCCFF enables 6.5% reduction in power compared to the full swing flip-flop with 19% area overhead. In addition, a frequency dependent delay associated with driving pulsed flip-flops with a low-swing sinusoidal clock has been characterized. The LS-DCCFF has 870 ps longer data to output delay as compared to the full-swing flip-flop at the same setup time for a 100 MHz sinusoidal clock. The functionality of the proposed flip-flop was tested and verified by using the LS-DCCFF in a dual-mode multiply and accumulate (MAC) unit fabricated in TSMC 90-nm CMOS technology. Low-swing resonant clocking achieved around 5.8% reduction in total power with 5.7% area overhead for the MAC.

Keywords: Delay, Flip-Flop, Low-Swing, Power, Resonant Clock.

I. INTRODUCTION

The clock distribution network (CDN) in digital integrated circuits distributes the clock signal which acts as a timing reference controlling data flow within the system. Since the clock signal has the highest capacitance and operates at high frequencies, the CDN consumes a large amount of total power in synchronous systems. Approximately 30%–50% of high performance processor power is consumed in the CDN [2]. The CDN and latches dissipate around 70% of the IBM POWER4 1.3 GHz microprocessor’s power [3]. Latest developments in integrated circuit design specifically in 3-D integration where multi-plane synchronization is required, lead us to believe that the power consumption of the CDN will remain at these high levels [4]. Resonant clocking enables the generation of clock signals with reduced power consumption. The traditional approach for LC resonant CDNs is to use the LC tank to drive the global clock distribution while the local square clock is being delivered through conventional buffers. However, around 66% of clock power is being dissipated in the last buffer stage driving the flip-flops [5], leading to minor power savings in LC globally-resonant locally-square CDNs. In order to achieve maximum power savings, the LC tank should drive the entire clock network (both global and local) without using intermediate buffers. This would require designing, modifying and understanding flip-flop performance with the sinusoidal clock signal generated in LC resonant networks.

C. Kim et al. [6] demonstrated that a low-swing square-wave clock double-edge triggered flip-flop has enabled 78% power savings in the CDN. Low-swing clocking would normally require two voltage levels, VDD and VDD_LOW. These voltage levels can be generated using one of two schemes: 1) dual-supply voltages and 2) regular power supply. The first scheme adds circuit and extra area complexity to the overall chip design and layout. However, it leads to a reduction in the number of clock network transistors which improves power savings [7]. The second scheme uses circuit methods to achieve low-swing. However, the design of low-swing buffers becomes challenging in the absence of a second power supply [7]. We have followed a similar approach to the one proposed in [5] in which the clock buffers are removed to allow the global and local clock energy to resonate between the inductor and entire clock capacitance including the receiving end flip-flops thus enabling maximum power savings. In addition, removing the clock buffers simplifies LC low-swing clocking since only reduced swing buffers are used at the flip-flop gate and not in intermediate levels within the clock tree [8].

In this paper, we introduce a low-swing differential conditional capturing flip-flop (LS-DCCFF) for use in low-swing LC resonant CDNs. As far as the authors know, this is the first application of low-swing clocking to LC resonant CDNs. In our approach, no additional power supply is
required to achieve low-swing clocking. We have characterized a frequency dependent delay associated with driving the pulsed flip-flop with a low-swing sinusoidal clock. We also provide measurement results from an integrated test chip fabricated in TSMC 90-nm CMOS technology. Furthermore, we report the power savings achievable through low-swing clocking. The remainder of this paper is organized as follows. An Existing System in Section II. Section III Proposed System. Section IV includes simulation and measurement results obtained. The conclusion of this paper is provided in Section V.

II. EXISTING SYSTEM

In complex VLSI, significant amount of power is consumed by the clocking networks. The global nature of clock distribution interconnects and increased parasitic with scaling further results in the increased power consumption. The CDN of microprocessor is typically divided into global and local clock distributions. The global clock distribution comprises a clock source and the wires and buffers needed to drive the clock source to the logic gates. The local clock distribution network comprises of wires that connect to the clock loads-latches and gates- in the microprocessors functional units. Reducing the supply voltage is an attractive approach to reduce power but has a quadratic effect on power consumption. However, we need to decrease the transistor threshold voltage for scaling down the supply voltage. This leads to substantial increase in leakage power. In addition, decreasing the supply voltage would increase system susceptibility to variations. As a result, there is an increasing demand for power reduction schemes that do not require a reduction in the supply voltage.

By ensuring a constant path to VDD the effect of charge sharing is minimized. This is done by properly sizing the PMOS transistors. A short evaluation interval occurs after the rising edge of the clock when both the clock and inverted clock signals applied to transistors MN1/MN2 are above the threshold voltage level of the NMOS transistor. This type of flip flop design uses full swing clocking. By modifying this circuit and using low-swing clocking system we shall reduce the power consumption. The next section gives a detailed view of low-swing system.

III. PROPOSED SYSTEM

The clock distribution network (CDN) in digital integrated circuits distributes the clock signal which acts as a timing reference controlling data flow within the system. Since the clock signal has the highest capacitance and operates at high frequencies, the CDN consumes a large amount of total power in synchronous systems. Approximately 40%–50% of high performance processor power is consumed in the CDN. The CDN and latches dissipate around 60% of the IBM POWER 1.4 GHz microprocessor’s power. Latest developments in integrated circuit design specifically in 3-D integration where multi plane synchronization is required, looking forward to believe that the power consumption of the CDN will remain at these high levels. Resonant clocking enables the generation of clock signals with reduced power consumption. The traditional approach for LC resonant CDNs is to use the LC tank to drive the global clock distribution while the local square clock is being delivered through conventional buffers. Therefore, around 66% of clock power is being dissipated in the last buffer stage driving the flip-flops, leading to minor power savings in LC globally-resonant locally-square CDNs. In order to achieve maximum power savings, the LC tank should drive the entire clock network (both global and local) without using intermediate buffers.

To analysis the correct operation of the proposed LF-DCCFF and to highlight potential power savings enabled through low/full-swing clocking, a test chip with a MAC unit designed using the proposed flip-flop under low/full-swing sinusoidal clocking was fabricated in TSMC 180-nm CMOS technology. Since the 16*16-bit multiplier itself was not pipelined, a clock frequency of 100 MHz was chosen for the test chip. Due to the large inductor needed for clock generation and the limited area available, the clock generator was not implemented on-chip. The sinusoidal clock signal is fed by an external source through an analog pad. Furthermore, the DCCFF was modified to enable dual-mode operation of the MAC unit under full- and low-swing clocking without significant area overhead. As illustrated, the LF-DCCFF presented was modified at node X to allow the operation under full- and low-swing clocking, it acts as an output path while executing. When signal FULL_SWING is high, full-swing clocking is enabled and the inverted clock output of the normal inverters CLKD_FS is feeding transistor MN1. Whereas low-swing clocking is enabled when signal FULL_SWING is low and the output of the reduced voltage swing inverters CLKD_LS feeds transistor. Two separate

Fig 1. DCCFF (full swing system).

The Differential Conditional Capturing Flip Flop (DCCFF) is shown in Fig. 1. Flip flop power is reduced at low data switching activities by eradicating unwanted transitions by a technique called conditional capturing. The DCCFF operates in a pre-charge and evaluate fashion. SET and RESET node’s are charged using pull-up PMOS transistors MP1 and MP2.
instances of the full- and low-swing DCCFF were implemented at the lower portion of the chip for testing. The overall area of the low/full-swing is taken from micro wind tool with TSMC 70nm technology. Finally the area of the swing is reduced.

IV. TEST CHIP EXTRACTED SIMULATION AND MEASUREMENTS

Fig.5 demonstrates the correct operation of the LS-DCCFF at a supply voltage of 1V with an operating frequency of 100 MHz and a low-swing sinusoidal clock. This figure shows the low-swing sinusoidal clock signal (channel 1, first signal from top), the inverted clock signal (channel 2, second from top), the input D (channel 3, third from top), and the output Q (channel 4).

HSPICE simulation on extracted circuits verifies correct functionality of both flip-flops under best conditions given by the Fast-Fast (FF) corner at a low temperature of -25°C, normal conditions given by the Typical-Typical (TT) corner at room temperature, and worst conditions given by the Slow-Slow (SS) corner at a high temperature of 125°C. An average reduction in the $T_{DQ}$ delay of 130 ps was observed in the FF corner whereas the SS corner resulted in 76 ps increase in delay compared to the TT corner. Furthermore, correct functionality of both flip-flops under low- and full-swing sinusoidal clocking with ±10% variation in the supply voltage was verified through measurements. A ±10% variation in low-swing clock results in 99 ps reduction and 300 ps increase in Hold time. Hold time reduces with higher clock swing due to a reduction in the delay of reduced swing inverters. The opposite is true for lower clock swing. The negligible variation in $T_{DQ}$ delay with clock swing is basically due to the change in the time required for the clock signal to reach $V_{pull-down}$. 

Fig.5. Measurement waveforms of the LS-DCCFF at 100 MHz
Post-layout-simulation results presented in Fig.6 illustrate that for the same setup time, the difference between the $T_{DQ}$ delays for the full and low-swing flip-flops is approximately 870 ps. This confirms the accuracy of with an error of 4% compared to simulation results for $V_{pull-down} = 500$ mV. The measurement results presented in the figure (limited by our experimental setup) are within close proximity to post-layout-simulation. The extra delay associated with measurements can be related to the extra capacitance of the pads, package, wires, and test fixture. The response presented in Fig.6 was obtained at the 0.5$V_{DD}$ voltage level for the data $D$ and output $Q$ waveforms and at half of the clock peak for the sinusoidal clock signals, i.e., at 0.5 and 0.325 V for the full- and low-swing clock signals, respectively.

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As illustrated in Fig. 6, $T_{DQ}$ becomes independent from $T_{DCLK}$ when data is applied on or after the point where the clock signal reaches or exceeds $V_{pull-down}$ since at this point transistors $MN1/MN2$ are completely switched on and are able to directly sink node $SET$ or $RESET$. This occurs in the full-swing case for a setup time less than or equal to 0 ps, i.e., when input $D$ is applied at or after point $T_1$. In the low-swing case, $T_{DQ}$ becomes independent from $T_{DCLK}$ when input $D$ is applied at or after point $T_2$, i.e., at a setup time less than or equal to -905 ps which is the time difference between the 0.325$V_{DD}$ and $V_{pull-down}$ for the low-swing sinusoidal clock signal.

| TABLE I: Area And Power Comparison Between Full-And Low-Swing Clocking |
|-----------------------------|-----------------|-----------------|
| Area (μm²)                  | LS-DCCFF        | MAC unit        |
| % Increase in area compared to full-swing | 19              | 5.7             |
| Power (μW)                  | 5.59            | 1,506           |
| % Decrease in power compared to full-swing | 6.5             | 5.8             |

Fig.6 also shows that the low-swing flip-flop can operate at a negative setup time of approximately -2000 ps whereas the full-swing flip-flop can only operate at a negative setup time of approximately -950 ps. This is because the reduced swing inverters in the low-swing flip-flop experience more delay than the normal inverters used in the full-swing flip-flop. Table I gives area and power overhead of low-swing as...
compared to full-swing resonant clocking. The area and power were estimated at the gate level. As shown in the table, the LS-DCCFF experiences 6.5% reduction in power as compared to the full-swing flip-flop with an area overhead of 19%. Static power consumption in the full-and low-swing flip-flops was assumed to be equal since the flip-flops have exactly the same transistor size except for the load pMOS in the reduced swing inverters. The table also illustrates that the application of low-swing clocking with the LS-DCCFFs causes a 5.7% increase in total area and 5.8% reduction in total power consumption.

The clock distribution network capacitance was estimated by using Cadence’s Calibre PEX extractor and then simulating the extracted net list in Cadence’s HSPICE simulator. Simulation results on the extracted network show that the clock net has a total capacitance of 8.48 pF. The inductor needed to resonate the clock network at 100 MHz is approximately 0.32 µH. Such a large inductor would normally be connected off-chip. In [10], the authors proposed a detailed analytical approach to determine required driver strength in the resonant clock based on the clock capacitance, resistance, output swing, and the pulse width of the applied reference signals. Using the approach proposed in [10], we illustrate that in order to resonate the clock tree at 100 MHz with a full-swing sinusoidal clock, the width of the pMOS transistor in the driver would be approximately 3.97 µm. To generate the low-swing clock signal with a reduced peak voltage of 0.65Vdd, the size of the transistor in the clock generator can be reduced by 66%. The scheme proposed in [12] in which a power management system based on automatic amplitude control can be used to insure the integrity of the generated clock with the desired peak voltage.

FIG 9.

VI. CONCLUSION

We have proposed a low-swing sinusoidally clocked flip-flop to obtain further power reduction in LC resonant CDNs. Low-swing resonant clocking in pulsed flip-flops results in a delayed flip-flop response. Theoretical analysis has been performed and the delay associated with low-swing sinusoidal clocking was characterized. The functionality of the proposed flip-flop has been investigated through HSPICE simulation on an extracted circuit layout at extreme corners and tested through on-chip measurements. A MAC unit designed using the proposed flip-flop was tested on-chip where low-swing resonant clocking achieves around 5.8% reduction in total power with a 5.7% area overhead.

VII. REFERENCES