Enhancement Power Gating Technique in Deep Submicron Circuit

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Abstract: Design of complex arithmetic logic circuits considering ground bounce noise, noise immunity, leakage current, active power and area is an important and challenging task in deep submicron circuits. In this paper, a comparative analysis of high performance stacking power gating schemes is done which minimizes the leakage power and provides a way to control the ground bounce noise. The innovative power gating schemes such as stacking power gating, , diode based stacking power gating are analyzed which minimizes the peak of ground bounce noise in transition mode for deep submicron circuits. Further to evaluate the efficiency, the simulation has been done using such high performance power gating schemes. Leakage current comparison of NAND gate without power gating and with power gating scheme is done. Finally it is observed that the leakage current in standby mode is reduced by 87.14% over the conventional power gating. It is also found that in stacking power gating, the ground bounce noise has been reduced by 76.280/0 over the conventional power gating scheme. We have performed simulations using Cadence Spectre in a 90n standard CMOS technology at room temperature with supply voltage of IV. Finally, a detailed comparative analysis has been carried out to measure the design efficiency of high performance power gating schemes. This analysis provides an effective road map for high performance digital circuit designers who are interested to work with low power application in deep submicron circuits.

Keywords: Power Gating Schemes, Stacking Power Gating, Diode Based Stacking Power Gating, Leakage Power and Ground Bounce Noise.

I. INTRODUCTION

With the rapid progress in semi conductor technology, chip density and operation frequency have increased, making the power consumption in battery- operated portable devices a concern [2]. High power consumption reduces the battery service life. The demand for portable electronic devices is growing rapidly and due in large part to the development of wireless communication, is expected to continue to grow. This demand has generated great interest in low power design. As the technology is reducing further day by day, contribution of leakage power in total power consumption has become comparable to or more than dynamic power consumption. For 180nm technology, it contributes only 10% of the total power while in 90nm technology it is comparable to dynamic power consumption, and for 45nm or technology less than this, leakage power is more than the dynamic power. In battery operated devices, leakage power may cause serious problem, it reduces the battery life. So, for battery operated portable devices, along with high performance, low leakage power consumption is advised.

The most efficient way to reduce the leakage current in standby mode is by using the power gating schemes that uses large transistors, called sleep transistors, in series with the pull. Up and pull- down stacks to cut off the power supply rail from the circuit when the circuit is in standby mode.

Ground bounce, also known as simultaneous switching noise or delta noise, is a voltage glitch induced at power ground distribution connections due to switching current passing through either wire substrate inductance or package lead inductance associated with power or ground rails [4]. These voltages glitches or surge phenomena are proportional to Ld/dt [4]-[8]. Ground bounce noise is an important issue in the design of nanometer circuits and this inductive noise is also associated with clock gating [9]. Taking into account technology trends ground bounce due to internal logic has become an important issue in the design of high performance integrated circuits. This is mainly due to the increased speed and higher density in scaled- down technologies. Finally, the paper is organized as follows: Section II explains Noise Power Gating Techniques for FPGAS. Section III illustrates Low Leakage Low Ground Bounce Noise Reduction Aware Power Gating Techniques. Section IV gives the comparative analysis of simulation results and finally the paper is concluded in section V.

II. NOISE POWER GATING TECHNIQUES FOR FPGAS

Design complexity is increasing day by day in modern digital systems. Due to the reconfigurable architecture, low non recurring engineering (NRE) and ease of design Field Programmable Gate Arrays (FPGA) become a better solution for implementation.

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for managing increasing design complexity. They are very much suitable for the application that requires both performance and flexibility. For the past few years, FPGAs witnessed an increase in market shares by providing a fast time-to-market alternative for ASICs. Due to the scaling trends and to support re-configurability, FPGA uses more transistors which increase the leakage current. As we know that leakage power is proportional to the total number of transistor count and so leakage optimization of FPGA becomes one of the major design challenges for future FPGA technologies. The biggest challenge for FPGAs implemented in nanometer CMOS technologies is the increasing power dissipation and in particular, leakage power. Also, as we go down to technology ground bounce noise also become important metric of comparable importance to active power, delay and area for the analysis and design of battery operated devices. Traditionally, leakage power reduction in FPGAs has been overshadowed by an interest in reducing the dynamic power dissipation and improving the overall performance. Recently, several research projects have been conducted to mitigate the leakage power reduction in FPGAs. The most popular of these techniques employs dual Vdd, transistor sizing, dual Vth, body biasing, multi-threshold CMOS (MTCMOS), and input vector forcing.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30×increase in gate leakage. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further peak of ground bounce noise is possible with proposed novel technique.

The biggest challenge for FPGAs implemented in nanometer CMOS technologies is the increasing power dissipation and, in particular, leakage power and ground bounce noise. Leakage power dissipation exponentially increases with the CMOS process scaling and is expected to dominate the total chip power dissipation in deep submicro CMOS process. To mitigate the leakage problem, power gating is widely implemented to suppress the leakage power in standby mode. Sleep transistors (ST), which are used to gate the power, deteriorate the noise characteristic of the circuits because their drain to source voltage drop changes the virtual rails of the circuit. Furthermore, during the mode transitions: especially from sleep mode to active mode, the power gating schemes cause large power and ground bounce that greatly affects the reliability of the circuits nearby in a mixed signal design. It is therefore essential to consider using techniques such as power gating to address the problem of ground bounce in low-voltage CMOS circuits. Ground bounce noise is the voltage induced at the internal power/ground connections due to the switching currents passing through the parasitic inductance associated to the bonding and package lead wiring. Ground bounce noise has been a phenomenon traditionally associated to input/output buffers. Buffers are typically used to drive large capacitive loads. Due to this fact large currents flow through the parasitic inductance and significant voltage glitches are induced at the internal power/ground connections. Switching noise affects the performance of the integrated circuits. Taking into account technology trends ground bounce due to internal logic has become an important issue in the design of high performance integrated circuits. This is mainly due to the increased speed and higher density in scaled-down technologies.

Device targeted for mobile applications typically require standby currents in the range of 10’s to 100’s of μA. Current low cost FPGA’s consumes up to 100mW of standby power. So if we can decrease the leakage power of FPGA’s that it can be used for fast growing mobile IC applications. Also, by proper leakage power and ground bounce noise analysis of different deep submicron FPGA devices we can use them in low power wireless, biomedical and other battery operated devices applications. This paper focuses on reducing leakage power consumption and ground bounce noise of low power FPGA benchmark circuit using power gating scheme. We provide a design which did a significant reduction in standby leakage and ground bounce noise so that it can be used for battery operated devices.

III. LOW LEAKAGE LOW GROUND BOUNCE NOISE REDUCTION AWARE POWER GATING TECHNIQUES

A. Basic LUT Structure of Benchmark circuit

The fig. 1 shows the basic LUT design of benchmark circuit 74182. This design is considered as the conventional case for all comparisons. This section provides the different leakage current and ground bounce noise reduction power gating techniques.

1. Stacking power gating technique

Here we present a benchmark circuit (fig.2) using stacking power gating technique. In this technique, stacking sleep transistors are used to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. In this technique, the leakage current is reduced by the stacking effect, turning both MSL1 and MSL2 sleep transistors off. Here, we apply the SELECT input in a manner by which the ground bounce noise is minimum this is achieved by adjusting the value of AT (this is the delay introduced to the SL signal using delayed buffer) which gives
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the summation of ground bounce noises of these two transistors minimum. When the value of $\Delta T$ is half of the oscillation period of the ground bounce noise then the positive peak of the ground bounce noise superimposes with the negative peak thereby bringing it closer to zero.

Fig.1. Look Up Table of benchmark circuit 74182 (Conventional case).

2. Diode based stacking power gating technique

If we incorporate the strategy which is operating the sleep transistor as a diode in stacking power gating leads diode based stacking power gating. Stacking sleep transistors (T1, T2) are used in diode based stacking power gating scheme shown in fig.3 reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. The diode based stacking power gating scheme consists of 5 parts:

1. Transistors T1, T2 are the sleep transistors which are high Vt transistors for less leakage current.
2. Transistor S1 is a control transistor used to make the sleep transistor S1 working as a diode during mode transition.
3. TG1 is the transmission gate.
4. Tn time delay provided for T1 and T2.
5. C2 is the capacitor inserted in the intermediate node VGD2.

Fig.2. Look Up Table with stacking power gating technique.

Fig.3. Lookup Table with diode based stacking power gating technique.

In this scheme, 3 strategies have been used to reduce the peak of ground bounce noise and leakage current.

1. Making the sleep transistor working as a diode during mode transition for some period of time due to this limitation in large transient hence reduction in the peak of ground bounce noise.
2. Isolating the ground for small duration during mode transition this was achieved by delay circuitry.
3. Turning ON the T2 transistor in linear region instead of saturation region to decrease the current surge was achieved by a capacitor placed in intermediate node.

There are several benefits of combining stacked sleep transistors with capacitors. First, the magnitude of power supply voltage fluctuations/ground bounce noise during mode transitions will be reduced because these transitions are gradual. The leakage current is reduced by the stacking effect, by turning both T1 and T2 sleep transistors off whereas, in terms of peak of ground bounce noise the technique works in two stages.

1. In first stage sleep transistor T1 works as diode by turn on the control transistor S1 which is connected across the drain and gate of the sleep transistors T1. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wakeup time. In sleep to active transition mode, we are turning on transistor T1 initially, after small duration of time transistor T2 will be turned on to reduce the ground bounce noise.
2. In second stage control transistor is off so that sleep transistor works normally. During mode transition, T1 is
turned on and transistor T2 is turned on after a small duration of time Tn.

3. Diode based staggered phase damping power gating technique
This technique can be understood by fig.4. The analyzed diode based staggered phase damping scheme consists of 5 parts:
1. Transistors T1, T2 are the sleep transistors which are high Vt transistors for less leakage current.
2. Transistors CT1, CT2 are the control transistors used to make the sleep transistors working as a diode during mode transition.
3. SG1, SG2 are transmission gates.
4. DIP-40 package pin ground bounce noise model connected beneath of the clusters.
5. Cluster1 and cluster2 denote logic blocks.

Fig.4. Look Up Table with diode based staggered phase damping power gating technique.

This scheme works on two strategies.

**Strategy 1:** The sleep transistor works as a diode during mode transition for some period of time. Due to this there is a reduction in large transient current hence reduction in the peak of ground bounce noise.

**Strategy 2:** During standby-to-active mode transition, we delays the activation time of one of the two sleep transistors relative to the activation time of the other one by a time that is equal to half the resonant oscillation period. As a result, noise cancellation occurs.

Two clusters have been taken to apply the technique. This technique provides a controllable path between the gate and drain of the sleep transistors SG1 and SG2. The turn–off and turn on of the control transistors CT1 AND CT2 make the sleep transistors work in the normal operation, the control transistors are turned off and has no impact on the sleep transistors. When the circuit is going from sleep to active mode, there exists a two stage procedure. The two stage procedure is common for both the sleep transistors but operate with a time delayed by half the oscillation period. We delays the activation time of one of the sleep transistors relative to the activation time of the other one by a time that is equal to half the resonant oscillation period. In stage I, the transmission gate SG1 is turned off and the sleep control signal is cut off, the input node of the sleep transistor SG1 is a floating node. And at the same time, the control transistor CT1 is turned on to make sleep transistor SG1 working as a diode.

The stored charge in the cluster1 is discharged through the sleep transistor SG1. We follow the same procedure for the sleep transistor SG2 also. The noise induced by the first sleep transistor SG1 is similar to that induced by the second sleep transistor with a phase shift. This phase shift suppresses the overall power mode transition noise. And same signals are applied to second cluster2 also but with duration of half of the oscillation period as calculated. As a result, noise cancellation occurs once the second sleep transistor SG2 turns on due to phase shift between the noises induced by the second transistor hence reduction in peak of ground bounce noise.

IV. COMPARATIVE ANALYSIS OF SIMULATION RESULTS

A. Simulation setup with stacking power gating scheme with basic NAND gate, including ground bounce noise
The complete simulation setup has been done with basic NAND gate including ground bounce noise model with stacking power gating scheme. Here the effectiveness of the stacking power gating scheme has been demonstrated using NAND gate circuits (fig 5).
"1". Hence the leakage current in this case is maximum for 2-input NAND gate. When the input vector sequence is "00" pull down transistors are turned OFF due to stacking effect, hence the leakage current is reduced. All the mentioned results have been simulated under condition that all the logical inputs of NAND gate circuit are held at logic '1'. The worst case condition has been taken where leakage current is maximum, to show the effectiveness of the stacking power gating scheme. To show the improvement in leakage reduction, the stacking power gating scheme has been compared with conventional power gating scheme in terms of leakage current and power dissipation.

**C. Leakage Current and power Comparison**

The tradeoff between leakage current and power supply in power gating can be easily analyzed from the graph mentioned in the leakage current comparison of NAND gate without power gating scheme and with stacking power gating scheme (fig 6). The leakage current in standby mode is reduced by 87.14% over the conventional power gating scheme shows comparison of the average leakage power dissipation in standby mode over the duration of 10 sec, for the conventional and stacking power gating schemes. It is analyzed that variation of leakage power dissipation with supply voltage is minimized in the stacking power gating schemes. Here a high performance stacking power gating schemes have been analyzed which minimizes the leakage power as well as control the ground bounce noise in transition mode. The tradeoff between the ground bounce noise and wakeup latency has been explored for high performance power gating circuits. As recent trend is towards the nano-scale regime, power gating scheme is mostly used for reduction of leakage current. The ground bounce noise caused by the power gating structure is getting more prominent as the supply voltage is scaled down from 1.5V to 0.5V. The modified stacking power gating scheme reduces the leakage current by 87.14% and ground bounce noise by 76.28% compared to the conventional power gating structure.

![Fig.6. Trade off between leakage current and supply voltage in power gating.](image)

**TABLE 1: Roadmap for Power Gating Schemes For Low Leakage Low Ground Bounce Noise Nanometer Logic Circuits**

<table>
<thead>
<tr>
<th>High Performance Power Gating Schemes</th>
<th>Applications</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stacking Power Gating</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- This scheme improves the wakeup latency penalty by 26.21% over the conventional power gating scheme.</td>
<td></td>
<td>Minimizes the leakage power as well as control the ground bounce noise only in transition mode.</td>
</tr>
<tr>
<td>- In this scheme, leakage current in standby mode is reduced by 87.14% over the conventional power gating scheme.</td>
<td></td>
<td>This scheme improves the wakeup latency penalty by 26.21% over the conventional power gating scheme.</td>
</tr>
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<table>
<thead>
<tr>
<th>Diode based stacking power gating scheme</th>
<th>Achieves ground bounce reduction of 2.4x and 1.72x compared to stacking and conventional power gating schemes</th>
<th>More ground bounce reduction as on comparison with other schemes</th>
</tr>
</thead>
</table>

A comparative study is also done for leakage current and ground bounce noise reduction (fig 7). In this Diode based stacking scheme is analyzed as the best among the existing schemes and leakage current is found to be least in stacking
power gating scheme. This analysis provides an effective roadmap for high performance digital circuit designers who are interested to work with low power application in nanometer logic circuits. The penalty of using the stacking power gating scheme, diode based stacking power gating scheme which is also present in conventional power gating structure, is that the logic level of the circuitry is not retained during the sleep mode. Hence future works will be directed towards resolving this data retention issue.

The proposed and conventional power gating techniques provide the power supply system the ability to adjust the output power. The power consumption can be further reduced if the power supply system has the enhanced ability to adjust the output voltage level and low power in continuous manner. Research efforts are desired in developing such techniques. The penalty of using diode based staggered, diode based stacking power gating techniques or the conventional power gating structure are that the logic level of the circuitry is not retained during the sleep mode. Hence future works will be directed towards resolving this data retention issue. The input vector dependency on the proposed power gating techniques has to explore for the better performance of the circuit. We can effectively apply the proposed circuit-level power gating techniques to the system level, by using an efficient power management schemes.

The proposed and conventional power gating schemes for low leakage low ground bounce noise in Deep Submicron Circuits”, vol. 3, pp. 197-205, June 2008.

Fig.7. Leakage power comparisons with Stacking and conventional power gating.

V. CONCLUSION

Power gating is an effective method to reduce leakage current during the circuit sleep mode. However, the conventional power gating technique for minimizing leakage current introduces ground bounce noise during sleep to active mode transition. Here a high performance stacking power gating structure has been presented which will minimize the leakage power as well control the ground bounce noise in transition mode. Stacking power gating technique has been analyzed and the conditions for the important design parameters (i) Minimum ground bounce noise have been derived. As recent trend is towards the nano-scale regime, power gating scheme is mostly used for reduction of leakage current. The ground bounce noise caused by the power gating structure is getting more prominent as the supply voltage is scaled down from 1.5V to 0.5V. The modified stacking power gating scheme reduces the leakage current by 87.14% and ground bounce noise by 76.28% compared to the conventional power gating structure.

In stacking power gating scheme when ΔT= 0, 9nSec minimum ground bounce of 112.04V is achieved. At ΔT= 0, 2nSec minimum wakeup latency 1.1 nSec being achieved at the cost of high peak of ground bounce noise 330μV At ΔT= 0, 7nSec peak of ground bounce noise is 21 0. 8μV. Trade off has been done between leakage current and supply voltage in order to obtain optimum performance. Innovative power gating structures are also presented which reduces the peak of ground bounce noise in transition mode. The diode based staggered power gating technique, has been implemented on inverter chain. By using this diode based staggered power gating technique, peak of ground bounce noise when it is applied to identical clusters. In case of diode based stacking power gating technique, reduction in peak of ground bounce noise is about 1.72 times compared to stacking power gating technique. The penalty of using the stacking power gating technique, which is also present in conventional power gating structure, is that the logic level of the circuitry is not retained in sleep mode. Hence future works will be directed towards resolving this issue.

VI. REFERENCES

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