Implementation of 3G WCDMA Systems Using Cyclic Hierarchical Code

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Abstract: In 3G asynchronous WCDMA, the downlink receivers spent much time on acquisition and synchronization due to large computation time of the correlation and the detection of large codes (512) used. The work here deals with a reconfigurable FPGA design using VHDL hardware description language to provide realization of frame synchronization and code group identification to be complied with the 3GPP standard. The implementation is based on cyclic Hierarchical codes which show better cross correlation properties than that of CFRS (Comma Free Reed Solomon) codes. The proposed structure complexity is relatively low compared with that for CFRS: we need just one correlator instead of 16 and (32*16) ROM instead of (64*60) is required. A low complexity approximation is used to calculate the true magnitude of signals. Also different clock frequencies for correlation calculation are used. As a result, one slot is sufficient to obtain frame synchronization.

Keywords: 3G, Wcdma, FPGA, Xilinx, cyclic codes.

I. INTRODUCTION

First generation (1G) mobile communications systems were based on analog technology and started in the early to mid 1980’s. These 1G systems had a number of limitations which includes

1. Low quality voice service,
2. Limited capacity and
3. Inability to provide global roaming.

Digital second generation (2G) systems were then developed in Europe and US. The various second generation systems includes

1. Global System for Mobile communication (GSM) which utilizes time division multiple access (TDMA). In TDMA each user is assigned a particular time slot.
2. The TDMA/136 specification which was defined in the US, in 1988, by the Telecommunications Industry Association (TIA), developed with the aim of digitizing the analog Advanced Mobile Phone Service (AMPS).
3. In the US, IS-95 was proposed for 2G systems, to provide better voice quality and higher capacity. IS-95 was based on CDMA technology. However, different 2G technologies were not interoperable and not available across geographic areas. In addition, the low bit rate of 2G systems could not meet subscriber demands for multimedia services.

Third generation (3G) systems aim to solve these problems encountered with 2G systems, by promising global roaming across 3G standards, higher data rates, improved quality of service and support for multimedia applications. The most popular candidates for 3G cellular systems are CDMA2000 and Wideband-Code Division Multiple Access (W-CDMA). Both of these schemes are based on Direct Sequence-Code Division Multiple Access (DSCDMA) technology. In DS-CDMA, the data signals are directly modulated by a digital code signal.

II. CELL SEARCH DESIGN

Cell search design is critical as it impacts the system performance and there is a need to design efficient receiver structures and algorithms to reduce the cell search time. This Chapter summarizes efforts by research groups and the 3GPP working groups to design efficient schemes...
and algorithms for each of the three stages of the cell search algorithm Wang et al. proposes a pipelined process to be used in first three stages of the cell search algorithm. The cell search scenarios considered in their study are

(1) Initial cell search: when a mobile is switched on and
(2) Target cell search: during idle and active modes of the MS.

Instead of the serial cell search sequentially searching through code, time and frequency, their method first acquires code and time synchronization assuming a larger frequency error and then performs frequency synchronization.

The synchronization code sequences used in stage 1 and stage 2 of the cell search algorithm are made up of bits called "chips" which can be either +1 or -1. The synchronization code sequences are 256 chips in length. If a traditional matched filter is used then a huge adder circuit (256 input adder) will be required to sum up the correlation results. This will lead to wastage of hardware resources. Hence, Siemens and Texas Instruments in their working group draft have suggested a hierarchical matched filter design which uses two matched filters to reduce the hardware complexity significantly.

A. Cell Search Algorithm

This Chapter describes the synchronization channels in W-CDMA cell search and introduces the cell search algorithm used in the synchronization of the MS with the BS for WCDMA systems.

B. Synchronization Channels in W-CDMA

In CDMA systems, spreading codes are used to differentiate physical channels from the same transmitter, and scrambling codes are used to differentiate transmitters. The MS needs to achieve code and time synchronization with the BS before any communication with the BS can start. The process of searching for a code and achieving synchronization with the BS is called cell search. Cell search is performed in two scenarios: when a MS is switched on (initial cell search) and during active or idle mode (target cell search). Target cell search is used to find handover candidates during a call. Cell search design is important and needs to be completed in minimum delay as it impacts the system performance. Each cell in a CDMA system is identified by its downlink scrambling code which is of length 38,400 chips.

Fig1: Synchronization Channels in Cell Search

The 38,400 chips form a radio frame which is divided into 15 slots. Each slot in the radio frame is of 2,560 chips. Figure shows the slot and frame structure of the three synchronization channels used in cell search: the Primary-Synchronization Channel (P-SCH), Secondary-Synchronization Channel (S-SCH) and the Common Pilot Channel (CPICH). The P-SCH together with the S-SCH are also called Synchronization Channel (SCH). In the P-SCH, a 256 chip sequence is transmitted at the start of each slot. The same P-SCH sequence is used by all the BSs and is transmitted once every slot. As the same sequence is used by all the transmitting stations, only one matched filter is sufficient to detect the slot boundary value. To reduce the complexity of the matched filter implementation, a hierarchical scheme is used as will be explained in detail in Chapter 4. The S-SCH is used for carrying 15 different sequences, one in each slot, for the different code groups and is repeated after every frame. These sequences are used in identifying the code group.

III. STRUCTURE OF SSCH USING CYCLIC CODES

In WCDMA (wideband code division multiple-access) cellular system, the procedure employed by a mobile station (MS) to search for the best cell site is referred to as cell search. A three-stage cell search scheme has been designed slot synchronization, frame synchronization with code group identification, and scrambling code identification. To
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facilitate cell search, three channels are used, namely the Primary Synchronization Channel (PSCH), the Secondary Synchronization Channel (SSCH), and the Common Pilot Channel (CPICH). The P-SCH together with the SSCH are also referred to as the Synchronization Channel (SCH).

During the first stage of the cell search procedure the MS uses the SCHs Primary Synchronization Code (PSC) to acquire slot synchronization to a cell. This is typically done with a single matched filter matched to the PSC which is common to all cells as shown in Figure. The slot timing of the cell can be obtained by detecting peak values in the matched filter output. The starting position of the synchronization code may be determined from observations over one slot duration. In the second stage, the secondary synchronization codes (SSCs) and comma free Reed Solomon (CFRS) codes are detected for frame synchronization and code group identification.

There are 16 SSCH sequences. In frame of 15 slots, 15 SSCH sequences create a code-word taken from code-book of 64 code-words. In each frame the same code word is transmitted in the cell. Code-group can be detected by identifying code-word. All 64 code-words are chosen to have distinct phase shift. After achieving slot synchronization, SSCH can be easily found. In the second stage, the receiver operation start with correlating the received signal of SCH with all possible SSC sequences (480 sequences) and identifying the maximum correlation value. Since the cyclic shifts of the sequences are unique, the code group as well as the frame synchronization is determined in this stage.

Table 1 Sequences X1i and X2i for Code Groups 1 to 32

<table>
<thead>
<tr>
<th>Code Group</th>
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<tr>
<td>1</td>
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<td>15</td>
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<td>16</td>
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The Secondary Synchronization Channel (SSCH) consists of 15 sequences of cyclic codes repeatedly transmitted in parallel with P-SCH. These 15 sequences belong to a family of cyclic codes each of length 256 chips (SSC). The cyclic hierarchical sequence CSI,k of the first slot is constructed from two constituent sequences X1i and X2i of length n1 and n2, respectively, using the formula:

\[ \text{CSI} (n) = X2i (n \mod n2) + X1i (n \div n2) \mod 2 \] ……(1)

where i is code group number

The constituent sequences X1i and X2i in each code group i are chosen to be identical, from Table 1, each of length 16 chips. X2 is the inner constituent sequence, X1 is the outer constituent sequence. Also, CSI, k of slot 1 (first slot) is referred to as the zero cyclic shift sequence as no shift is applied to the constituent outer sequence X1i. The procedure to construct the cyclic hierarchical sequences of slots 2 to 15 is from the two constituent sequences X1i, k-1 of length n1 and n2 respectively using the following formula:

\[ \text{CSI}, k (n) = X2i, k-1(n \mod n2) + X1i, k-1(n \div n1) \mod 2 \] ……(2)
where \( n \) is the chip number within the slot, \( n=0,1…n_{1}*n_{2} -1 \) 
\( i \) is the code group number, \( i= 1,2..... 32 \) 
\( k \) is the slot number, \( k = 2, 3…15 \)

The constituent sequence \( X_{1i}, k-1 \) (outer seq.) is formed by the base sequence \( X_{1i} \) using the cyclic shifts of \( X_{i} \) on \( k-1 \) positions (from 1 to 14). The constituent sequence \( X_{2i}, k-1 \) (inner seq.) is exactly equal to the base sequence \( X_{2i} \) in every slot, i.e.:

\[
X_{2i, k-1} = X_{2i} 
\] \( \text{for all } k \) \( \ldots \ldots \text{(3)} \)

The generation of the cyclic codes can be clarified clearly by considering the following example. \( X_{1,0} = (1,1,1,-1,-1,-1,1,1,1,-1,1,1) \)
\( k=1 \) for slot 1, no cyclic shift
\( X_{1,1} = (1,1,1,1,-1,-1,-1,1,1,1,-1,1,1) \)
\( k=2 \) for slot 2, right shift by 1 position.
\( X_{1,14} = (1,-1,-1,1,1,1,1,1,-1,1,1,1,1) \)
\( k=15 \) for slot 15 right shift by 14 positions.

The same procedure to form the cyclic codes will be used for other code groups. Hence, for 32 code groups and 15 slots, there will be 480 different cyclic hierarchical sequences of 256 chips length that can be constructed. These 480 (32*15) cyclic codes have good correlation properties which make them good candidates for SSCs. Many pairs of cyclic codes are fully orthogonal, some pairs have small cross correlation and only small percent (3-5%) have cross correlation values reaching up to 25% of the auto correlation value of the PSC. These 480 cyclic codes are unique for each code group/slot location pair. So, it is possible to uniquely determine both the scrambling code group and the frame timing in the second stage of the initial cell search.

IV. ARCHITECTURE DESIGN OF SSCH

Figure shows the SSCH cell search design (CSD). The input data samples of SSCH are stored in the SSCH buffer with 256 complex memory cells called buffer one (BF1) after the first stage complete detection of P-SCH, i.e. slot synchronization. The input data fills the 256 memory cells of BF1 using system clock timing. The secondary synchronization code is detected in four steps:

**Step-1:** The input data is stored in the 256 memory cells of BF1 divided into 16 block symbols of 16 bit each.

**Step-2:** Correlating the above blocks sequentially with inner constituent sequence X2 by the first parallel correlator (inner correlator) of the hierarchical matched filter as shown in Fig through multiplexer. The 16 correlation outputs of the first correlation stage are stored in shift register 2 (BF2) of the second parallel correlator MF (outer correlator).

**Step-3:** Correlating the stored outputs from step2 with the outer constituent sequence X2. This correlation is repeated 15 times with each right shift of X2 to detect the slot number.

**Step-4:** Repeat steps 2 and 3 for each of the 32 code groups stored in the ROM. The 32 cyclic codes are stored in a ROM according to table (1) and each is tried in succession before the data from the next slot comes in. The data in the shift register (BF1) is latched till all these sequences have been correlated.

This is achieved in stage-2 by using two clocks, once the data is latched in the buffer; the fast clock is used to perform the correlation (steps 2 & 3).

![Frame synchronization and code group](image-url)
Hence, one MF correlator is used to detect the SSC instead of 16 correlators which are necessary to decode the comma free sequences used by the 3GPP algorithm to detect code group and frame synchronization. This means a reduction in hardware of 15 MF correlators. This is the main advantage of the proposed design in the 3GPP cell search algorithm.

As shown in Figure., the proposed system consists of two buffer shift registers (256 registers each 8bit width) for I and Q, MUX1, inner corap (parallel correlator), DEMUX1, outer corap, magnitude calculator, peak searcher, 32x16 ROM, and the control circuit (cntrcct). The correlation results over Q and I channels are combined non coherently over one slot duration. This noncoherant combiner used here is called magnitude approximate. Keeping in mind that, the most important information of the peak detection is not the peak itself, but its location. On the other hand, for coherent combiners, the main operations are multiplications (squaring) used to calculate the true values of signals. In cell search, the most important information of magnitude values calculation are just used to compare with each other for finding the largest one and hence to detect its location.

Hence a magnitude approximation is sufficient and avoids the use of multipliers. Normally, a simplification can be used by squaring both I and Q values and then summing to have the magnitude squared;

\[ P^2 = I^2 + Q^2 \]  
\[ \text{(4)} \]

The use of multipliers for squaring means high cost in simplification. A low-cost approximation is proposed. where : 

\[ P^2 = |a|^2 + |b|^2 \]  
\[ \text{(5)} \]

Thus only shift operations are needed. A magnitude squaring sub-module (mgseq) approximator is designed and implemented using FPGA. The timing control consists of three counters, two 16 bit counters operates alternatively and 32 bit address counter. The two 16 bit counters are counter and sft_cntr. The counter component controls the MUX (to transfer the 16 Buff blocks to cortap) DMUX (to transfer cortap output to cortap2 input), and starting of sft_cntr. After 16 block correlation,(from cortap)sft_cntr. Starts controlling the inner cortap operation. Outer cortap makes 15 correlation operations.

These correlations are performed without shifting of outer code, while the other14 are shifted (stored in sftreg). Hence as sft_cntr controls the shifting of outer cortap shfreg, it counts the number of shifts. Hence sft_cntr provides the slot number for the detected cell by step one. The frame synchronization can, therefore, be easily obtained. At count 16 of sft_cntr counter starts and a new code is loaded to both correlators from the ROM (32X16), which stores the SSC’s. The address counter output represents the code group number, which transferred to step three. Address counter output represents the code group number, which transferred to step three. Address counter increments by one with each 16 counts of sft_cntr. The peak searcher, non coherently, searches for the peak value. There are two correlation operations as described above for Incident(Isc) and Quadrature (Qsc) of the input data of SSCH.
V. CONCLUSION

A design of SSCH for 3G communications system using cyclic hierarchical codes is presented. The main design features are the configurability and flexibility. Also one slot search period time (0.67 ms for 2560 chips) is enough to uniquely identify the correct code group and the frame timing in the second stage of acquisition when the signal to noise ratio is high. This improves the 3GPP-comma free cell search algorithm, where at least three slots are necessary to uniquely identify the correct code group and frame timing. A smaller size ROM 32X16 is used compared with the 3GPP-comma free CSD which uses a ROM 64X60 to store the comma free codes. Also, 480 comparison candidates (32 X 15) is required instead of 960 (64 X 15) for 3GPP comma free CS. The architecture is completely designed and documented in synthesizable VHDL code. The architecture is synthesized using Spartan 3E FPGA. The performance of the synthesized architecture is sufficient to the most demanding applications of the third generation mobile receiver.

VI. REFERENCES

[1] Fpga – Based Fast Ssch Detector For 3g Wcdma Systems Using Cyclic Hierarchical Codes 2011 Ieee Gcc Conference And Exhibition (Gcc), February 19-22, 2011, Dubai, United Arab Emirat.


[5] 3gpp Ran Ts 25.213 V4.0.0 (2001-03) Technical Specification Group Radio Access Network: Spreading And Modulation (Fdd), (Www.3gpp.Org, Release 4). Figure (3): Configurable Parallel Correlator “Cortap” Component Figure(4): Frame Synch’ Behavioral Test Timing Diagram Figure.


