Abstract: In the electronics and communication decoding and encoding of any data(s) using VLSI technology requires low power, less area and high speed constrains. Viterbi decoder using survivor path necessary parameters for Wireless Communication to reduce the power and cost at the same time increasing the Speed Compared to normal decoder. In this paper the Gate Diffused Input Logic (GDIL) based viterbi decoder is designed using Xilinx ISE, simulated and synthesized successfully. GDIL viterbi provides very less path delay with low power simulation results. Our Proposed Technique which comprises a Survivor Path Unit (SPU) implements a trace back method with DRAM is again Compared with GDIL Viterbi. The viterbi decoders are compared, simulated, synthesized and the proposed approaches shows the best simulation and synthesize results for low power and high speed application in VLSI design. The Add-Compare-Select (ACS) and Trace Back (TB) units and its sub circuits of the decoder(s) have been operated in deep pipelined manner to achieve high transmission rate. All the designing of viterbi is done using Xilinx ISE 12.4 and synthesized successfully in the FPGA Vertex 6 target device operated at 64.516 MHz clock frequency reduces almost 41% of total path delay.

Keywords: Viterbi Decoder, GDIL Technique, SPU, DRAM, Pipeline, Add Compare Select (ASC), Trace Back (TB), Xilinx, FPGA.

I. INTRODUCTION

The Viterbi decoding algorithm, proposed by Viterbi, is a decoding Process for convolution codes in Memory-less noise. The algorithm can be applied to a host of problems encountered in the design of communication systems. The Viterbi Algorithm finds the most-likely state transition sequence in a state diagram, given a sequence of symbols. The Viterbi algorithm is used to find the most likely noiseless finite-state sequence, given a sequence of finite-state signals that are corrupted by noise. Generally, a viterbi decoder consists of three basic computation units: Branch Metric Unit (BMU), Add-Compare-Select Unit (ACSU) and Trace Back Unit (TBU). The BMU calculates the branch metrics by the hamming distance or Euclidean distance and the ACSU calculates a summation of the branch metric from the BMU and previous state metrics, which are called the path metrics. After this summation, the value of each state is updated and then the survivor path is chosen by comparing path metrics. The TBU processes the decisions made in the BMU and ACSU and outputs the decoded data. The feedback loop of the ACSU is a major critical path for the viterbi decoder. The decoding procedure compares the received sequence with all the possible sequences that may be obtained with the respective encoder and then selects the sequence that is closest to the received sequence. There are always two paths merging at each node and the path selected is the one with the minimum hamming distance, the other is simply terminated. The retained paths are known as survivor paths and the final path selected is the one with the continuous path through the trellis with a minimum aggregate hamming distance.

II. RESEARCH WORK

Y. Zhu and M. Benaissa (2003) presented a novel ACS scheme that enables high speeds to be achieved in area efficient viterbi decoders without compromising for area and power efficiency. Multilevel pipelining has been introduced into the ACS feedback loop. Arkadiy Morgenstern et al (2004) used Gate Diffusion Input circuits for asynchronous design and compared the designs with CMOS asynchronous design. Dalia A. El-Diband Mohamed I. Elmasry (2004) discussed the implementation of a viterbi decoder based on modified register-exchange (RE) method. Song Li and Qing-Ming Yi (2006) proposed a scheme based on Verilog language for the implementation of high-speed and low power consumption bi-directional viterbi decoder. The decoding was done in both positive and negative direction and the delay was half of that of the unilateralism decoder and the decoding speed was greatly improved. Yun-Nan Chang and Yu-Chung Ding (2006) presented allow power design for viterbi decoder based on a novel survivor path trace mechanism. Lupin Chen et al (2007) presented a Low-power trace-back (TB) scheme for high constraint length viterbi decoder. Xuan-zhong Li et al (2008) discussed a high speed viterbi decoder which was based on parallel radix-4 architecture and bit level carry-save algorithm. Seongjoo Lee (2009) presented an efficient Implementation method for parallel processing viterbi decoders in UWB systems.
III. VITERBI BASED ON GDIL TECHNIQUE

Gate Diffusion Input Logic (GDIL) is a technique of low power digital for circuit design which allows reducing power consumption, delay and area of the digital circuit the basic GDIL cell is similar to the standard CMOS inverter, the differences are: 1. GDIL cell contains three inputs. 2. Bulks of both NMOS and PMOS are connected to N or P, so it can be randomly biased at contrast with CMOS inverter. It have four terminals G, P, N, D nodes. GDIL viterbi decoder consists of three blocks. They are Branch Metric Unit (BMU), Add Compare Select Unit (ACSU) and Survivor Memory Unit (SMU). All these blocks are designed using GDIL technology, simulated and synthesized using Xilinx ISE.

A. Branch Metric Unit

The first unit is called branch metric unit. Here the received data symbols are compared to the ideal outputs of the encoder from the transmitter and branch metric is calculated. Hamming distance or the Euclidean distance is used for branch metric computation. The branch metric unit takes the fuzzy bit and calculates the cost for each branch of the trellis.

B. Path Metric Unit

The second unit, called path metric computation unit, calculates the path metrics of a RTL Design of Branch metric unit stage by adding the branch metrics, associated with a received symbol, to the path metrics from the previous stage of the trellis (fig 1 and 2). The add-compare-select unit is the heart of the Viterbi algorithm and calculates the state metrics. These state metrics accumulate the minimum cost of ‘arriving’ in a specific state. The branch metrics are added to state metrics from the previous time instant and smaller sum is selected as the new state metric:

C. Path Metric Unit

The second unit, called path metric computation unit, calculates the path metrics of a RTL Design of Branch metric unit stage by adding the branch metrics, associated with a received symbol, to the path metrics from the previous stage of the trellis (fig 3). The add-compare-select unit is the heart of the Viterbi algorithm and calculates the state metrics (fig 4). These state metrics accumulate the minimum cost of ‘arriving’ in a specific state. The branch metrics are added to state metrics from the previous time instant and smaller sum is selected as the new state metric:
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IV. TRACE BACK METHOD

The TB method, the storage can be implemented as RAM and is called the path memory. Comparisons in the ACS unit and not the actual survivors are stored. After at least L branches have been processed, the trellis connections are recalled in the reverse order and the path is traced back through the trellis diagram (fig 5).

![Image](image1.png)

**Figure 5. Trace back unit.**

V. SYNTHESIS REPORT OF PROPOSED VITERBI

The developed proposed viterbi is simulated and verified its functionality. Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE 12.4. In synthesis process, the RTL model will be converted to the gate level netlist mapped to a specific technology library (fig 6). This modified viterbi decoder design is implemented on FPGA (Field Programmable Gate Array) family of Virtex 6. Here in this Virtex 6 family many different devices were available in the Xilinx ISE tool. In order to implement this modified viterbi with DRAM, the device named as “XA9536XL” has been chosen and the package as “FG320” with the device speed as “– 6 ”. The design of modified viterbi decoder for low power and high speed is synthesized successfully and its results are analyzed. After completion of synthesize the entire circuit model is processed through Translate, Map, Place and Route successfully. Finally a UCF file of the target object is created which is prototyped with hardware FPGA Virtex 6 hardware, through parallel connection using JTAG (fig 7). Boundary Scan is performed followed by generation of PROM file. Finally the modified viterbi with RAM cell is successfully configured into FPGA Virtex 6.

![Image](image2.png)

**Figure 6. Synthesis Report.**

**Figure 7. Configured into FPGA.**

VI. CONCLUSION

Viterbi decoding is the best technique for decoding the convolution codes. Viterbi decoder with constraint length 7 and code rate 1/3 has been developed. The main consideration is to decrease the power dissipation. The two techniques used for decoding the convolutional codes are the RE method and TB method. TB method is used for larger constraint length but takes more time for decoding. RE method is simplest and fastest but more suitable for small constraint lengths. The RE method with large constraint length (K=7) is implemented with Modified Register Exchange Method. This implementation reduces the power consumption to a large extent. The ACS unit and survivor memory management unit consumes most of the power. Bit serial approach is used for implementation of ACS unit. The amount of interconnections is reduced by using bit serial architecture and the butterfly concept unit which in turn reduces the power consumption. Further, power is reduced by using the modified register exchange method. Modified register exchange method uses the pointer concept. The extra overheads are the registers required for storing the carry bits and the path metrics.
VII. FUTURESCOPE
The Viterbi decoding is limited to lowering Constraint lengths. Viterbi decoder with Modified Register Exchange Method can be further investigated for higher constraint lengths.

VIII. REFERENCES