High Speed and Low Error Fixed-Width Modified Booth Multipliers for DSP Applications

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Abstract: In many high speed Digital Signal Processing (DSP) and multimedia applications, the multiplier plays a very important role because it dominates the chip power consumption and operation speed. In DSP application, in order to avoid infinite growth of multiplication bit width, it is necessary to reduce the number of multiplication products. Accuracy can be improved by way of modifying the partial product matrix of Booth multiplication and subsequently deriving an effective error compensation function. In addition, a simple compensation circuit composed of basic gates, derived from sorting network is also proposed for further improvement of accuracy. Compared to the direct truncated fixed width multiplier (DTFM), the proposed fixed width multiplier requires very less hardware. The generated partial products addition is implemented using CSA tree for minimization of the delay and area. The experimental results on two real life applications also demonstrate that the proposed fixed width multipliers can improve the average peak signal to noise ratio of output images by at least 2.0 db and 1.1 db respectively and also reduces power consumption and area.

Keywords: Error compensation circuit, Fixed-width multiplier, Mean error, Mean-square error, Modified Booth-multiplier.

I. INTRODUCTION

Multipliers are always the fundamental arithmetic unit and significantly influence the system’s performance and power dissipation. To achieve high performance the modified Booth encoding which reduces the number of partial products by factor of two through performing the multiplier recoding has been widely adopted in parallel multipliers. Significant hardware complexity reduction and power saving can be achieved by directly removing the adder cells of standard multiplier for the computation of the n least significant bits of 2n-bit output product. However, a huge truncation error will be introduced to this kind of direct-truncated fixed-width multiplier (DTFM). To effectively reduce the truncation error, various error compensation methods, which add estimated compensation value to the carry inputs of the reserved adder cells, have been proposed. Error compensation value can be produced by the constant scheme or the adaptive scheme. Even though it has the advantage of simplification, the truncation error of the constant scheme is relatively large. Adaptive scheme was developed to achieve higher accuracy than the constant scheme through adaptively adjusting the compensation value according to the input data at the expense of a little higher hardware complexity.

However, most of the adaptive error compensation approaches are developed only for fixed-width array multipliers but not used for fixed-width modified Booth multipliers. To overcome this problem, the compensation value was generated by using statistical analysis and linear regression analysis. This approach can significantly decrease the mean error of fixed-width modified Booth multipliers, but the maximum absolute error and the mean-square error are still large. To obtain better error performance with a simple error compensation circuit, Booth encoded outputs are utilized to generate the error compensation value.

In this paper, we propose a high-accuracy error compensation circuit for the fixed-width modified Booth multiplier. The circuit makes the error distribution not only be symmetric to but also centralize in zero error as much as possible. Therefore, the mean and mean-square errors can be significantly reduced simultaneously so that the resultant fixed-width multiplier is suitable for different applications whose output data may be produced from a single multiplication or multiply-accumulation operations. To accomplish this goal, we first slightly modify the partial product matrix of Booth multiplication to reduce the partial product bits in the truncated portion of DTFM. Then, the correlation between Booth encoded outputs and the truncated product error of DTFM is analyzed and explored to derive an effective and simple error compensation function, which can produce an approximation to the carry value generated by truncated portion of DTFM, to reduce the truncation error and make the error distribution as symmetric and centralized as possible. Finally, a simple...
compensation circuit composed of a simplified sorting network and some adder cells is developed according to the proposed error compensation function.

II. BOOTH MULTIPLIER EXPLANATION

![Booth Multiplier Figure](image)

**Algorithm:**

1. Pad the LSB with one zero.
2. Pad the MSB with 2 zeros if n is even and 1 zero if n is odd.
3. Divide the multiplier into overlapping groups of 3-bits.
4. Determine partial product scale factor from modified booth 2 encoding table.
5. Compute the Multiplicand Multiples.
6. Sum Partial Products

**TABLE 1: BOOTH ENCODING**

<table>
<thead>
<tr>
<th>$B_{2i-1}$</th>
<th>$B_{2i}$</th>
<th>operation</th>
<th>Neg$_i$</th>
<th>Two$_i$</th>
<th>One$_i$</th>
<th>Zero$_i$</th>
<th>Cor$_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>+0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>+A</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>+A</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>+2A</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-2A</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-A</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-A</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Booth Multiplication Example:

$$2AC9 \times 006A = 11010101011001001$$

**Explanation:**

1. Multiplicand (mp) = 2AC9
2. Multiplier (mr) = 006A
3. Applying two’s complement of Multiplicand.
4. Append one zero to LSB and two zeroes to MSB of multiplier.
5. Divide multiplier into overlapping group of three bits such that each group contains one bit of previous group.
6. Encode the multiplier according to the booth encoded truth table.
7. Compute the partial products.
8. Add partial products and remove the carry.

III. DIRECT TRUNCATED FIXED WIDTH MULTIPLIER (DTFM)

The Direct Truncated Fixed Width Multiplier achieves significant hardware complexity reduction and power saving can be achieved directly removing the adder cells of standard...
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Fig. 2. Partial product matrix for 8 * 8 modified Booth multiplication.

However, a huge truncation error will be introduced to this kind of direct truncated fixed width multiplier. The mean and mean square error will be very large. The truncation error is very large and unacceptable for many applications.

Drawbacks:

1. High power consumption.
2. Low accuracy.
3. Truncated error will be more.
4. Transmission Bandwidth will be high.

IV. FIXED WIDTH MODIFIED BOOTH MULTIPLIER (FWMBM)

The Fixed Width Multiplier is attractive to many multimedia and Digital Signal processing systems which are desirable to maintain a fixed format and allow a little accuracy loss to output data.

To reduce the truncation error, we first slightly modify the partial product matrix of booth multiplication using SC (Signal Conditioning)-generator and then derive an effective error compensation function. Compared to previous method, the proposed error compensation circuit can achieve a tiny mean error and a significant reduction in mean square error. The smaller mean error and mean square error represent that the error distribution is more symmetric to and centralized in the error equal to zero (denoted as zero error).

The above is Block Diagram of Booth Multiplier, Where Multiplier is Y and Multiplicand is X. Both X and Y is connected to the Booth Encoder. The purpose of Booth Encoder is used to generate the partial products. The compensation circuit is used to reducing the errors. The Carry Save Adder (CSA) used to adding the partial products and saving the carry value. The parallel prefix adder is used to adjusting stage and also adding the partial products. The final product is getting through the \( p_q \).

V. ERROR COMPENSATION CIRCUIT

SC-Generator: The term SC-Generator is nothing but signal conditioning generator, the purpose of SC-Generator is to check whether it is more number of 0’s or 1’s are present in the network.

Circuit Explanation: The inputs of SC-Generator are Zero \( i \) for \( 0 \leq i \leq n/2-1 \) and it will generate \( m \)-output bits \( \alpha_1, \alpha_2, \ldots, \alpha_m \) as shown in above fig. Where \( m= (n/2-1)/2 \) and \( s(\Phi) \) will be equal to \( \alpha_1+\alpha_2+\ldots+\alpha_m \). Due to the subtraction operation in \( [(R-1)/2]\), it is difficult to generate \( \alpha_1, \alpha_2, \ldots, \alpha_m \) by adder cells directly. Instead of adder cells, the proposed SC-generator is composed of a sorting network based on the following observation. We assume that zero \( i \) for \( 0 \leq i \leq n/2-1 \) can be sorted and the sorted outputs are \( p_i \) for \( 0 \leq i \leq n/2-1 \). Moreover, if the largest bits are gathered to the less significant positions, then \( \alpha_k=p_{2k} \) for \( 1 \leq k \leq m \). That is the problem of designing a SC generator can be translated into the design of a sorting network that sorts \( Zero_{n/2-1} \ldots \ldots Zero_{1}Zero_{0} \) into \( p_{n/2-1} \ldots \ldots p_1p_0 \) and \( \alpha_k=p_{2k} \).

Fig: 3. Block Diagram of Modified Booth Multiplier.

Fig: 4. The inputs and outputs of proposed SC-generator.
Error performance:

Explaination: There are 2 kinds of well known comparison based sorting networks, the bitonic and the odd-even merge sorting networks suited to hardware implementation. Since the odd-even merge sorter has the same number of compare levels as the bitonic sorter but requires fewer comparators, thus we adopt and simplify the odd-even merge sorting network to realize the SC-generator. Figures 6(a) and 6(b) illustrate the odd-even merge sorting networks for the case of n=8 respectively.

Explanation: The above figure illustrates the final partial product matrix of proposed fixed width modified booth multiplier for n=8. In it, all the partial product bits in LP'_{\text{minor}} are removed and replaced by the SC generator. In addition, the carries generated by LP'_{\text{minor}} are also replaced by the outputs of SC generator.

Advantages:

i) Low power consumption.

Application:

i) Real-time signal processing.

ii) Audio signal processing.

iii) Video/image processing.

VI. SIMULATION AND SYNTHESIS RESULTS
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The proposed method and existing method are simulated and synthesized by using Modelsim and Xilinx. The design summary of both are given below. Device utilization summary report is presented below. The Xilinx power analyzer gives the power value and this is calculated for both existing and proposed method and is listed below. The area and power comparison graph is also given. The error performance is also analyzed for both methods and are compared.

A. Existing method

<table>
<thead>
<tr>
<th>Logic utilization</th>
<th>used</th>
<th>available</th>
<th>utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Flip Flops</td>
<td>34</td>
<td>13,834</td>
<td>1%</td>
</tr>
<tr>
<td>Number of 4 input LUTs</td>
<td>208</td>
<td>13,834</td>
<td>1%</td>
</tr>
</tbody>
</table>

Total equivalent gate count for design: 2,021.
Additional JTAG gate count for IOBs: 3,312

Power report:

B. Proposed method
Total equivalent gate count for design: 561.
Additional JTAG gate count for IOBs: 1,584.

Power report:

![Power report](image)

**Summary:**
- Voltage [V]:
  - 1.8
- Current [mA]:
  - 712
  - 1230
- Power [mW]:
  - 1500
  - 2700

**Total Power:**
- 46.43 mW

**Battery (Operating Time):**
- 500.00 mAh
  - 6.00 mAh

**Battery (Life in Hours):**
- 0.00

**Power summary:**
- Total estimated power consumption: 46 mW
  - Vccint 1.80V: 22 mW
  - Vccio3 3.3V: 2 mW
  - Inputs: 4 mW
  - Logic: 2 mW
  - Outputs: 1 mW
  - Signals: 2 mW
  - Quiescent Vccint 1.80V: 15 mW
  - Quiescent Vccio3 3.3V: 2 mW

**Thermal summary:**
- Estimated junction temperature: 26°C
- Ambient temp: 25°C
- Case temp: 25°C
- Theta J-A: 17°C/W

**Decoupling Network Summary:**
- #
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TABLE I.
ERROR CALCULATION

<table>
<thead>
<tr>
<th>Pattern</th>
<th>x</th>
<th>y</th>
<th>Actual</th>
<th>DTFM</th>
<th>Proposed</th>
<th>DTFM Error value</th>
<th>Proposed Error value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>011</td>
<td>011</td>
<td>11111</td>
<td>11110</td>
<td>1000000</td>
<td>1111110</td>
<td>202</td>
</tr>
<tr>
<td></td>
<td>101</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
<td>0000000</td>
<td>54</td>
</tr>
<tr>
<td>2</td>
<td>011</td>
<td>011</td>
<td>00000</td>
<td>00000</td>
<td>0000000</td>
<td>0000000</td>
<td>236</td>
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<tr>
<td></td>
<td>010</td>
<td>010</td>
<td>11110</td>
<td>10000</td>
<td>0000000</td>
<td>0000000</td>
<td>20</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

The main Objective of this project is to reduce the number of partial products and truncation error by using the modified booth multiplier. In the proposed multiplier, the partial product matrix of Booth multiplication was slightly modified and an effective error compensation function was derived accordingly. This compensation function makes the error distribution be more symmetric to and centralized in the error equal to zero, leading the fixed-width modified Booth multiplier to very small mean and mean-square errors. Here the area and power is less compared to the previous method and the error value is also less.

VIII. REFERENCES


